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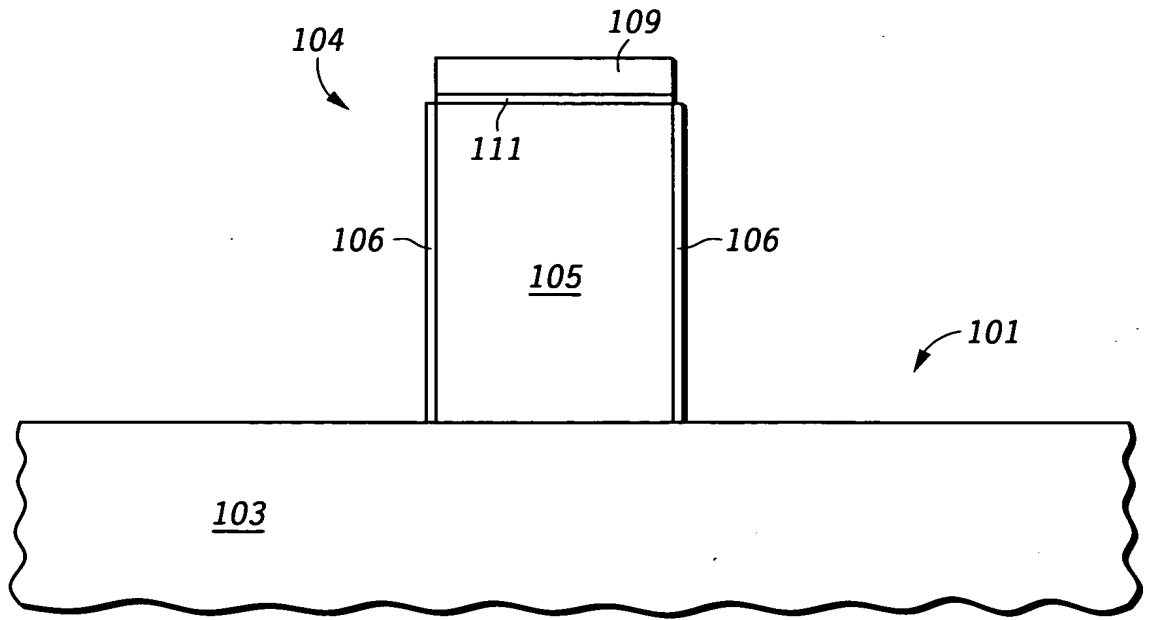


FIG. 1

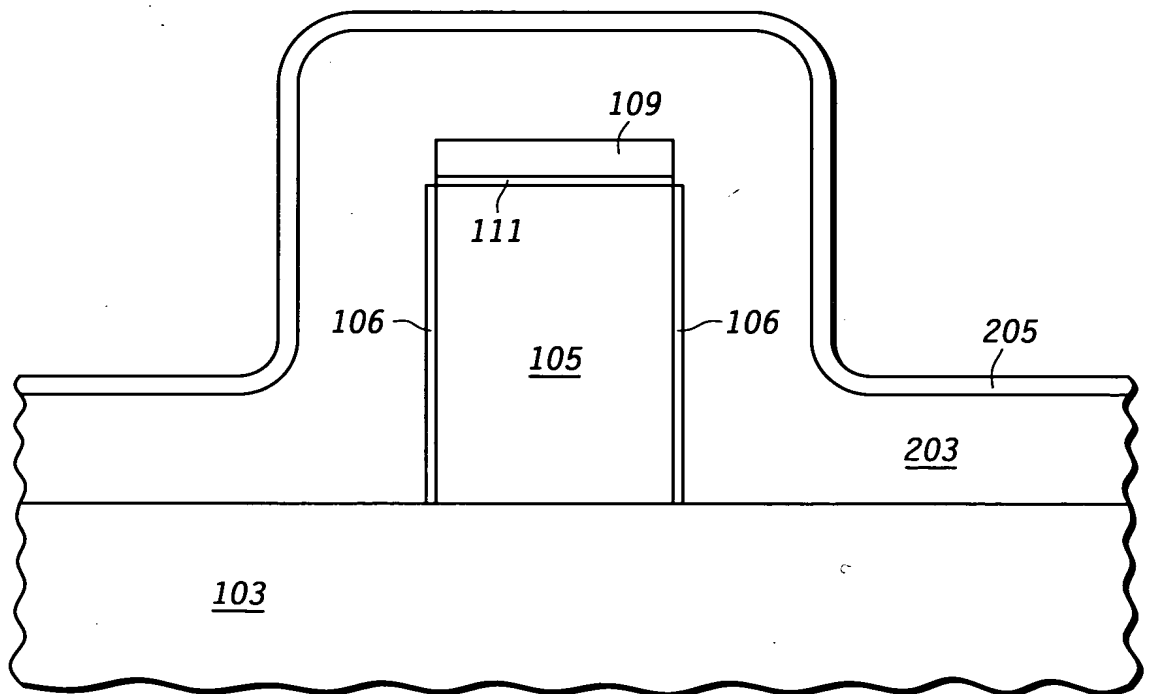


FIG. 2

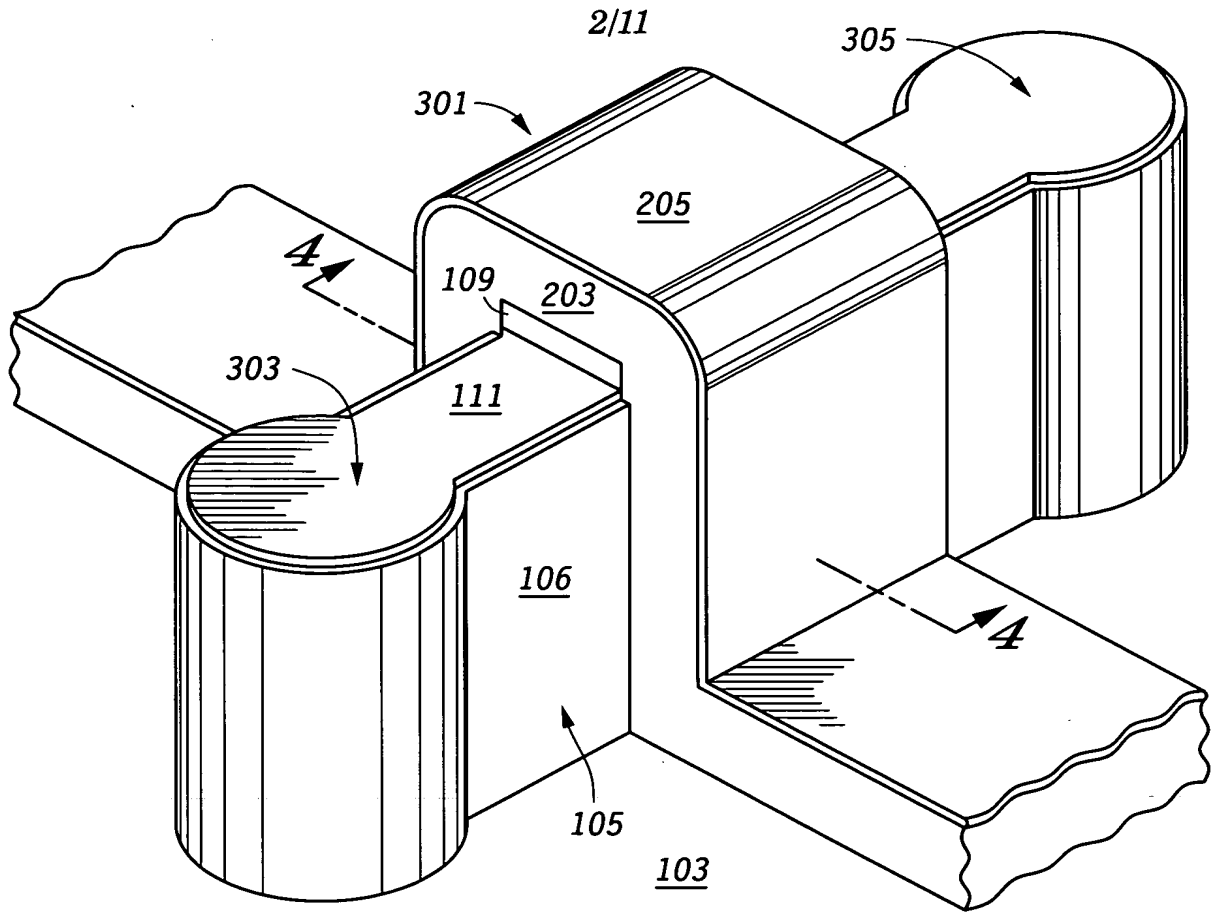


FIG. 3

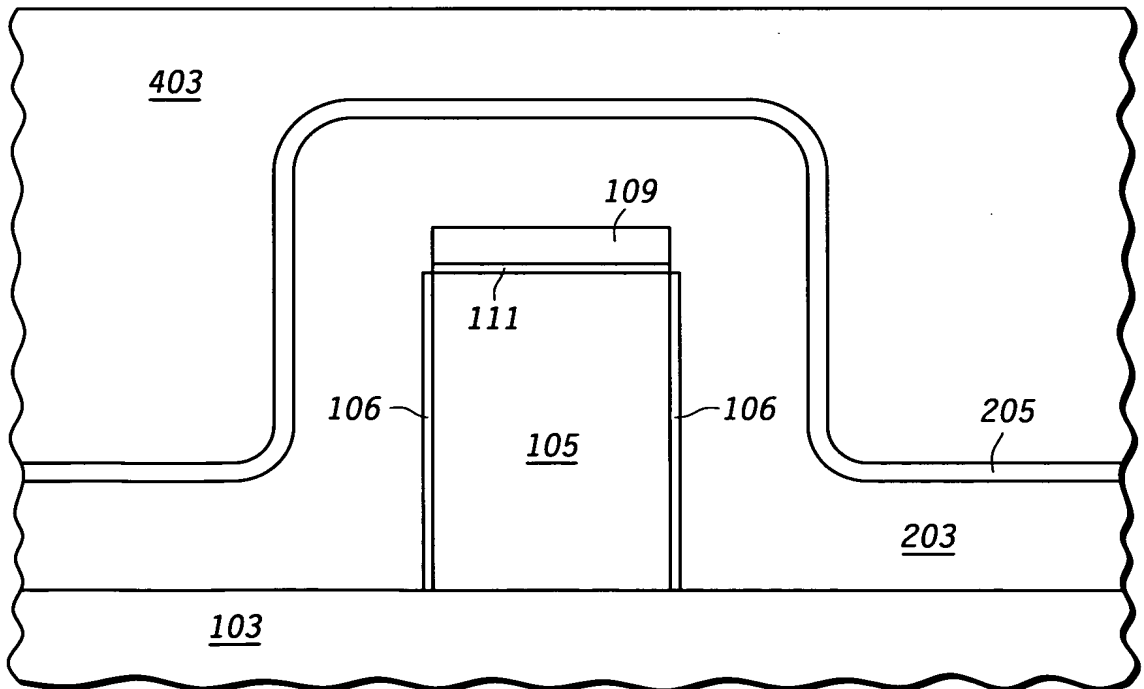


FIG. 4

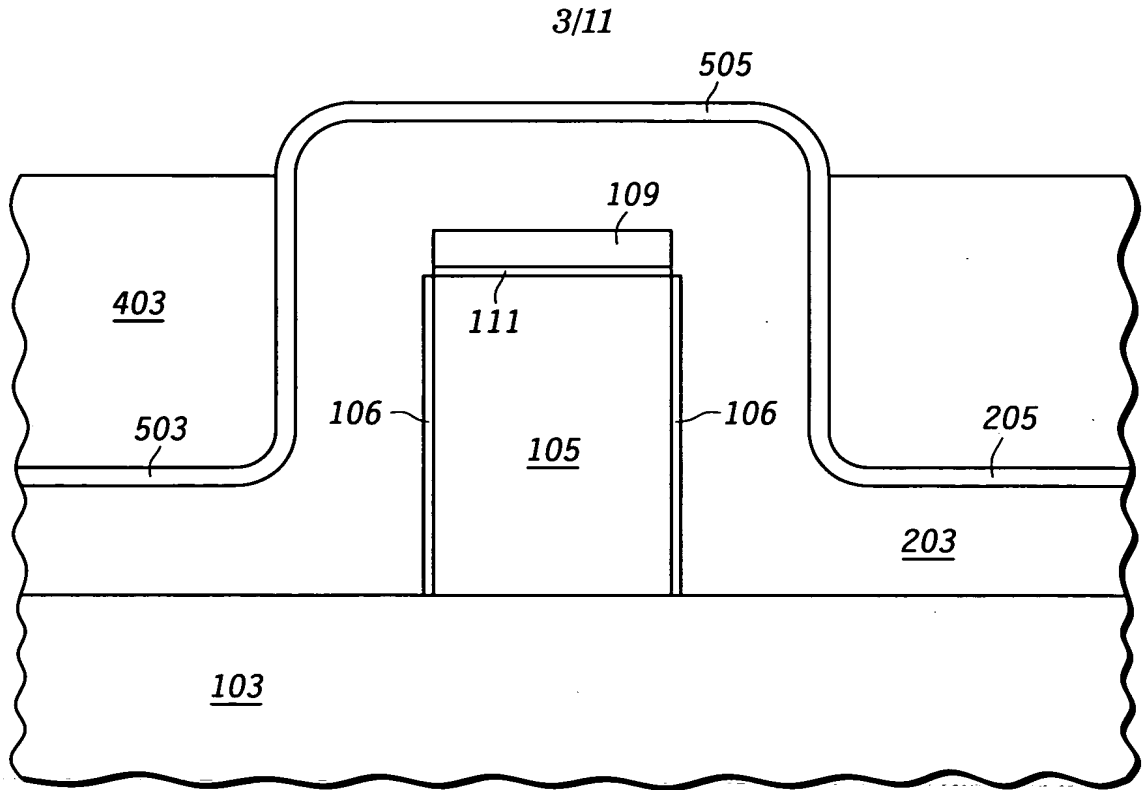


FIG. 5

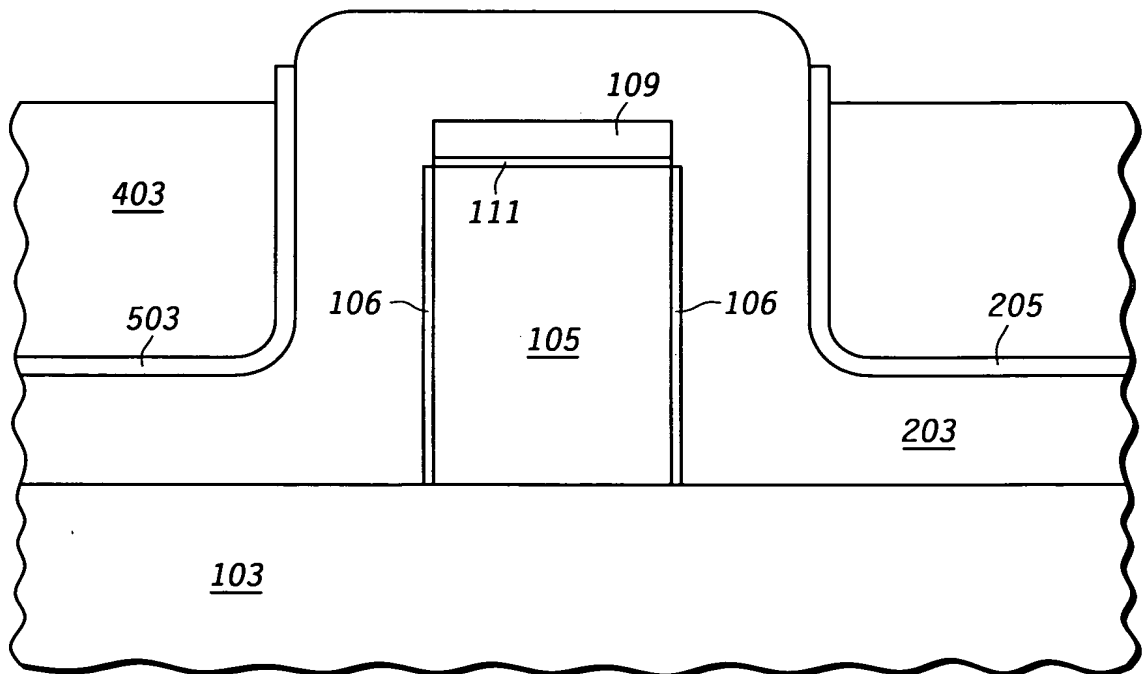


FIG. 6

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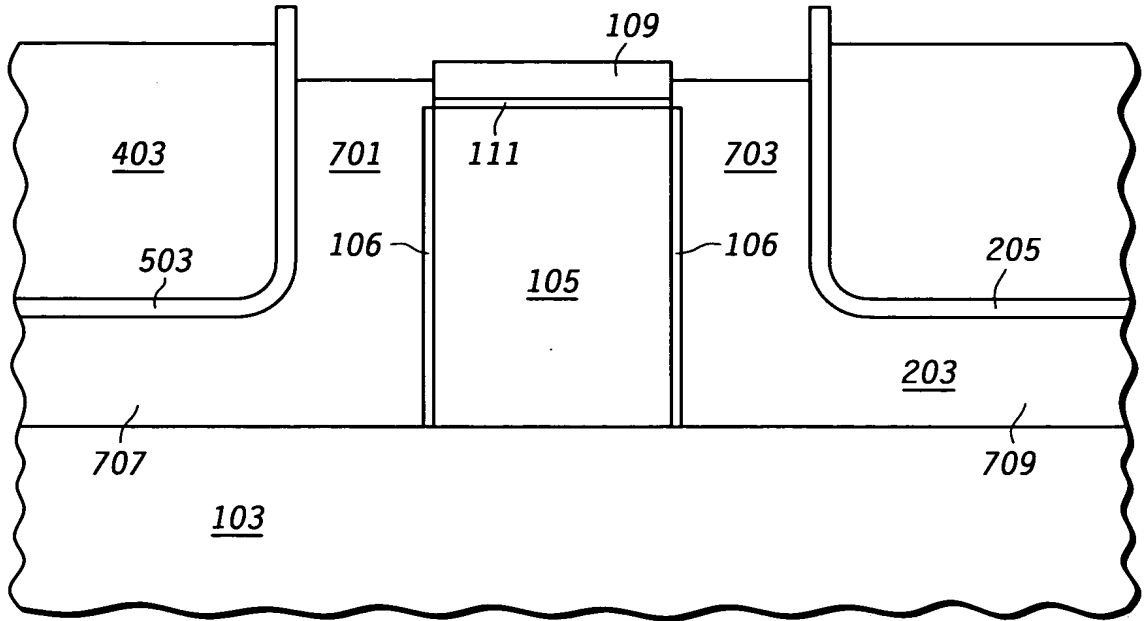


FIG. 7

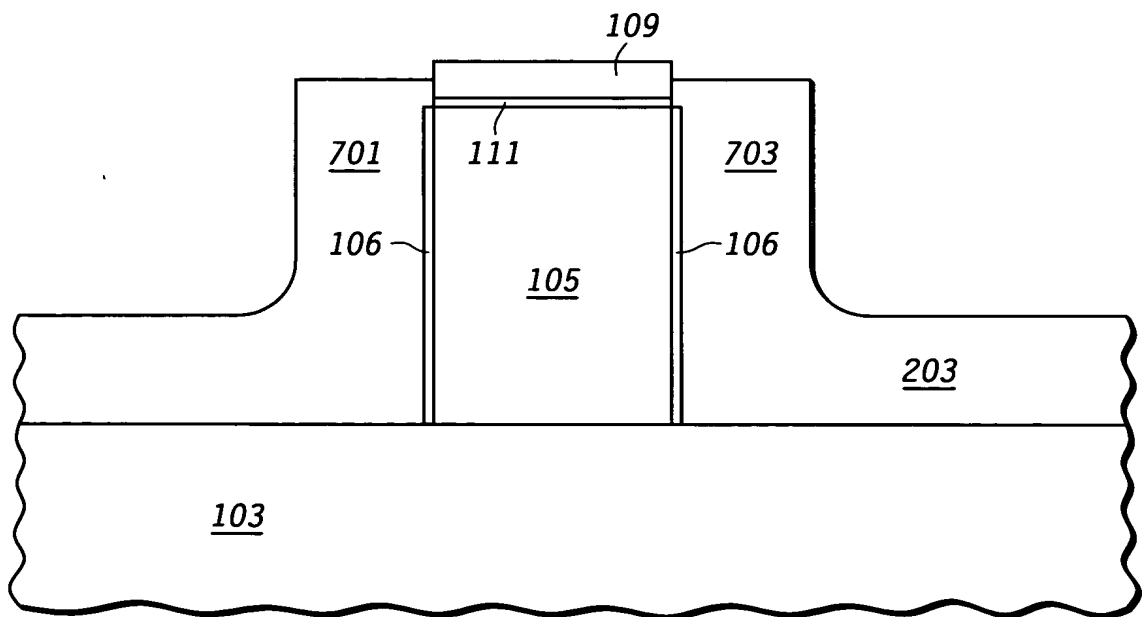


FIG. 8

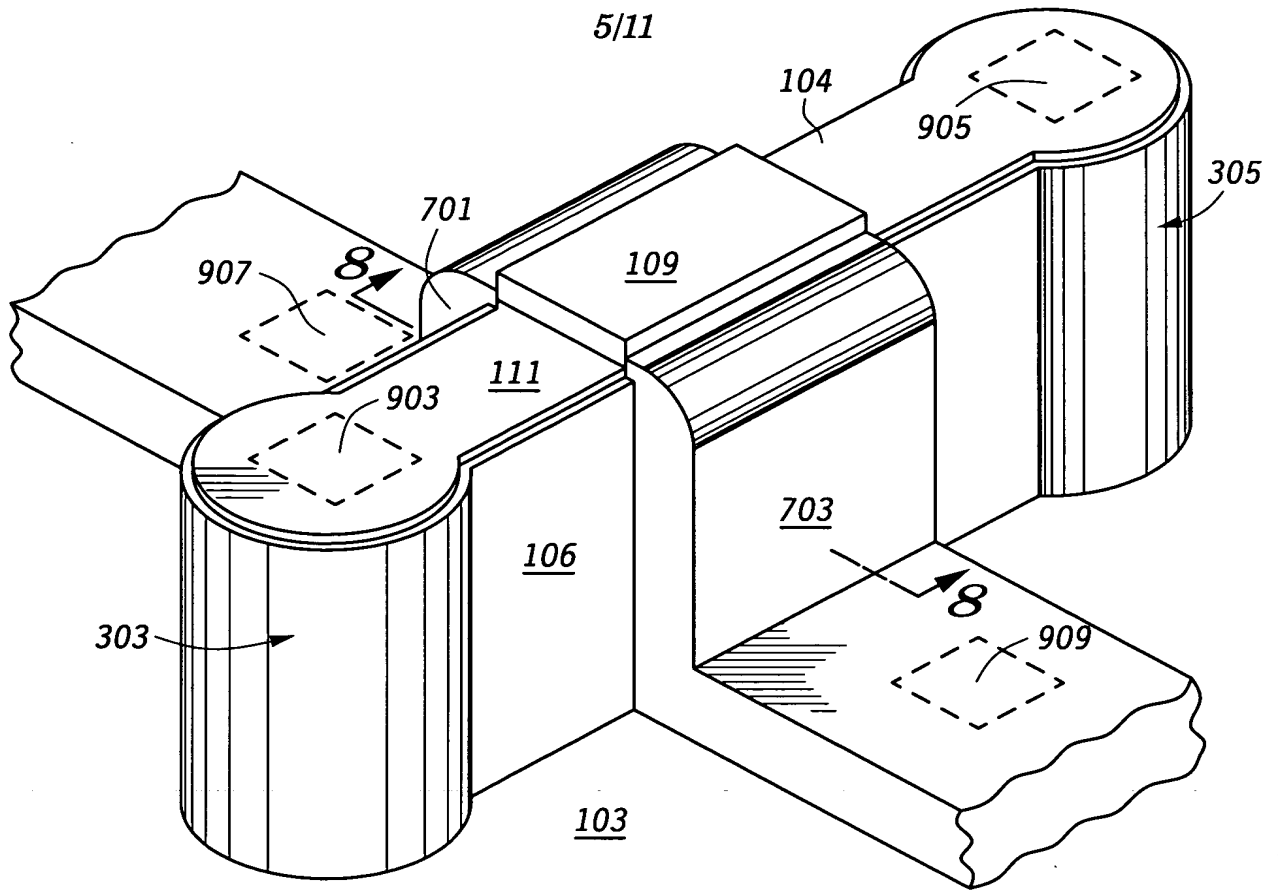


FIG. 9

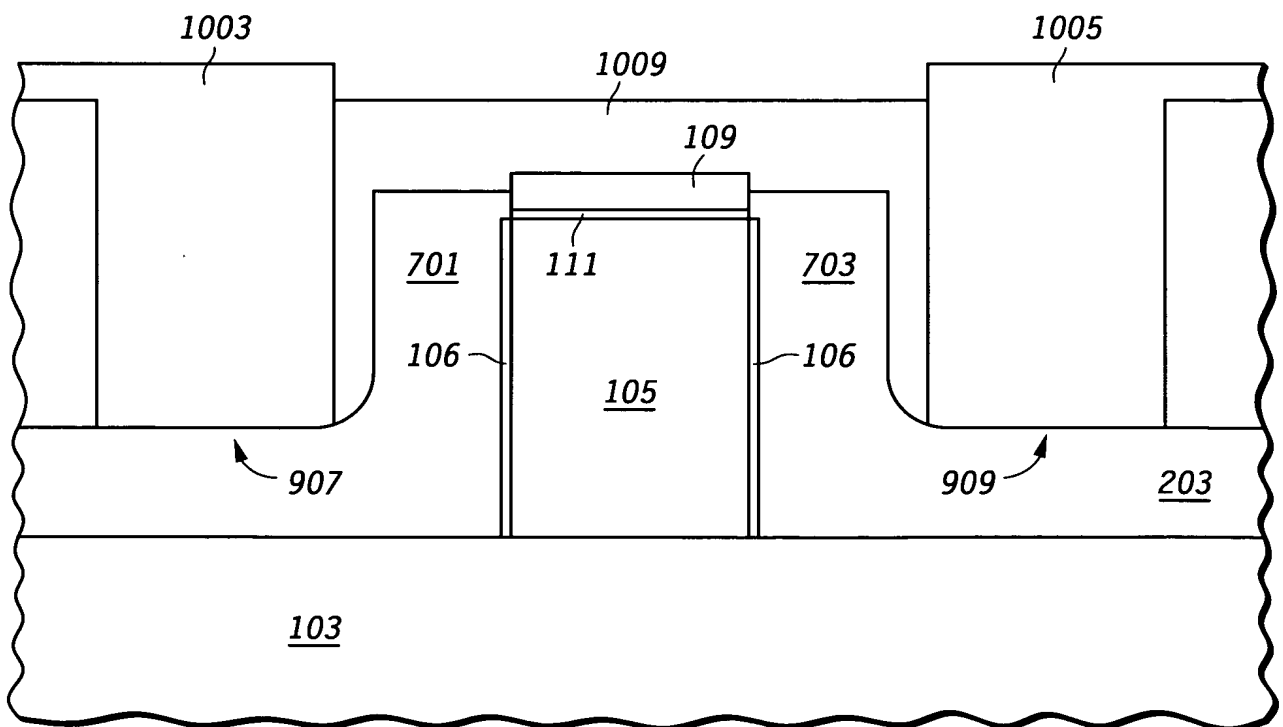


FIG. 10

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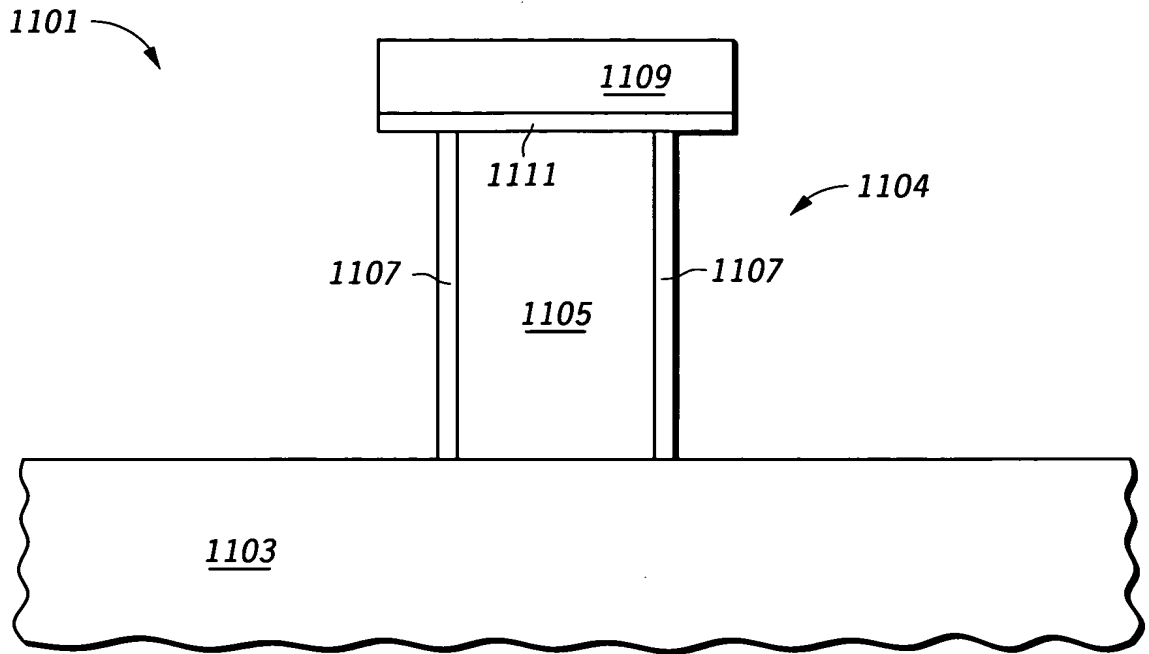


FIG. 11

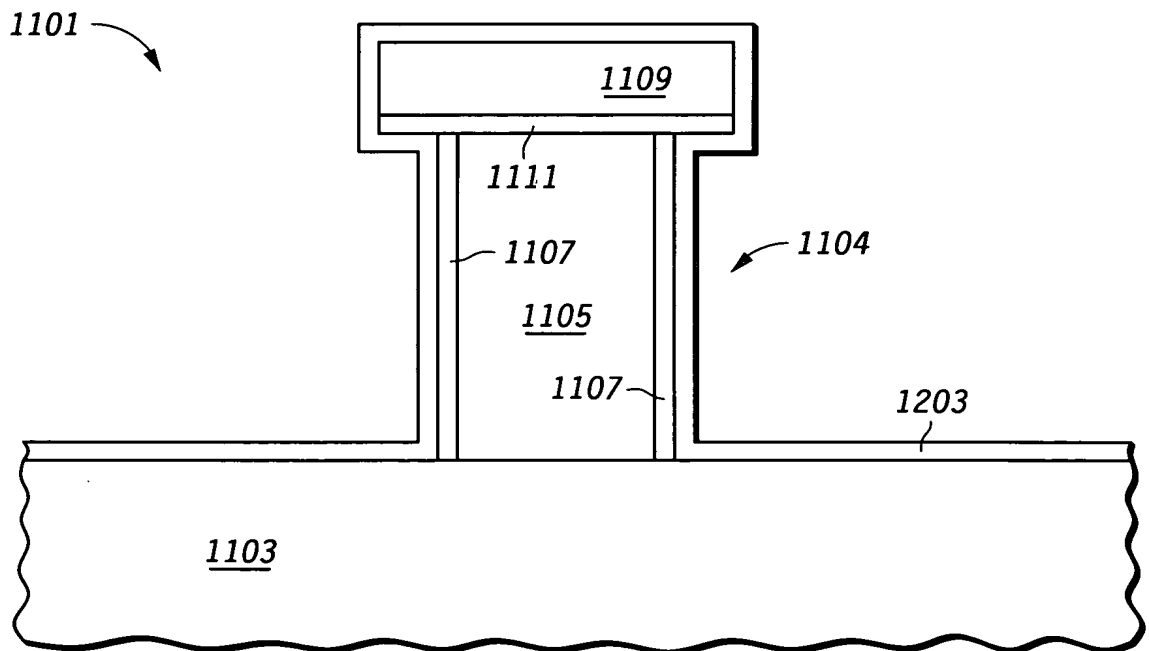


FIG. 12

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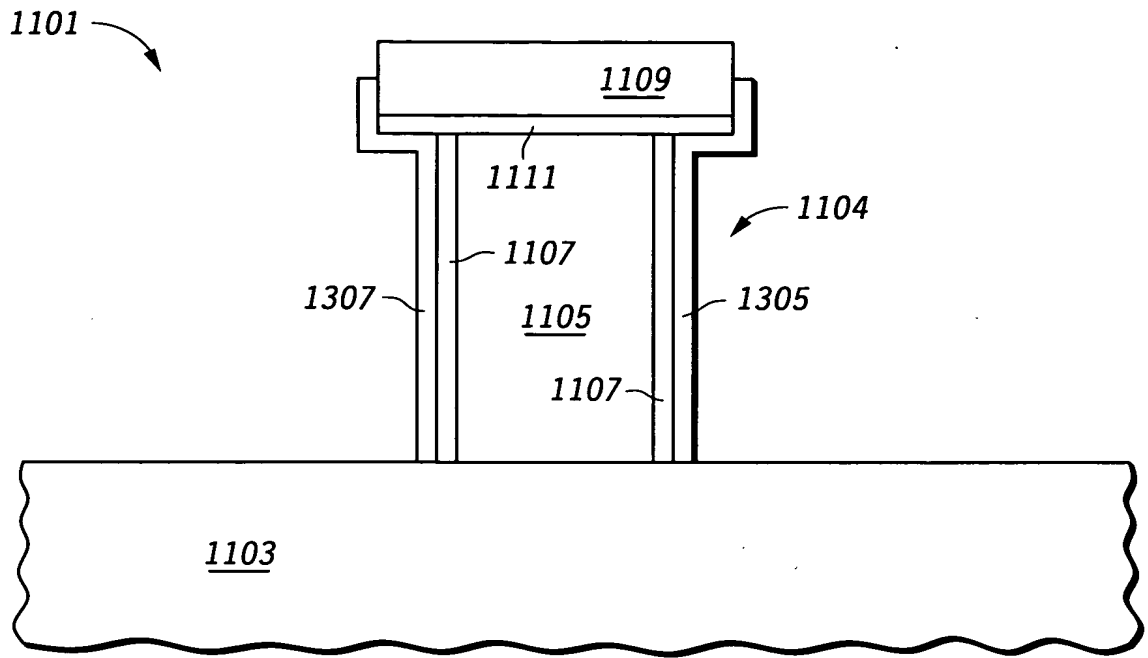


FIG. 13

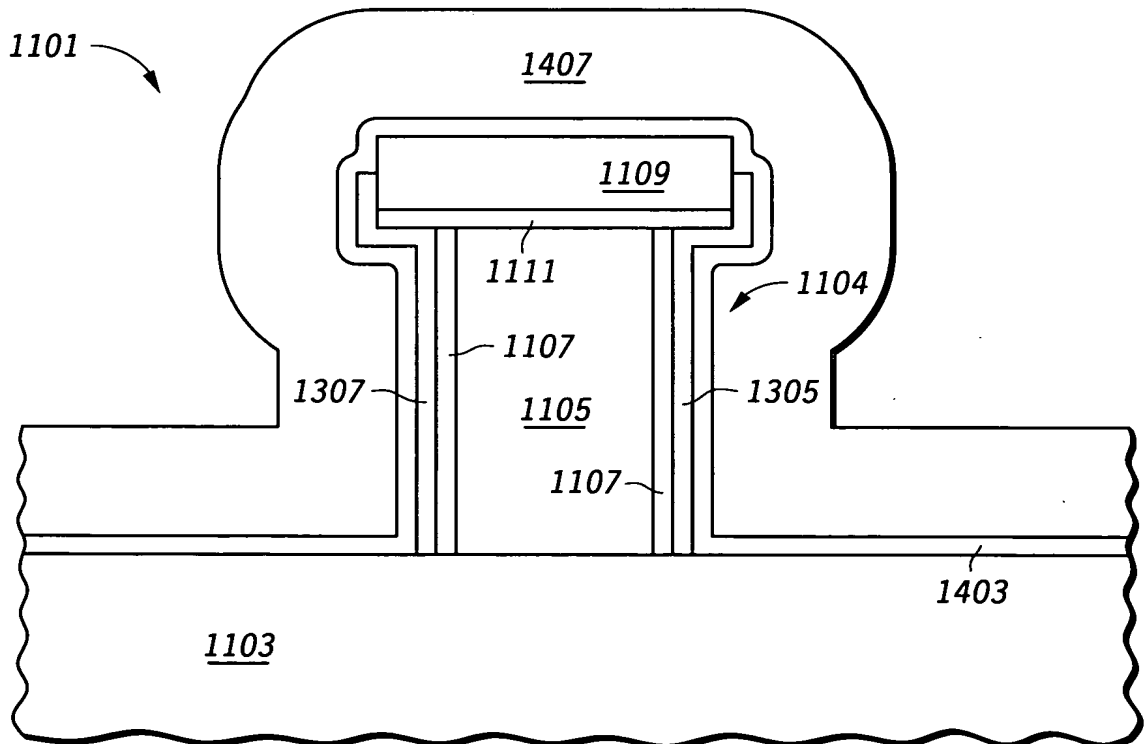


FIG. 14

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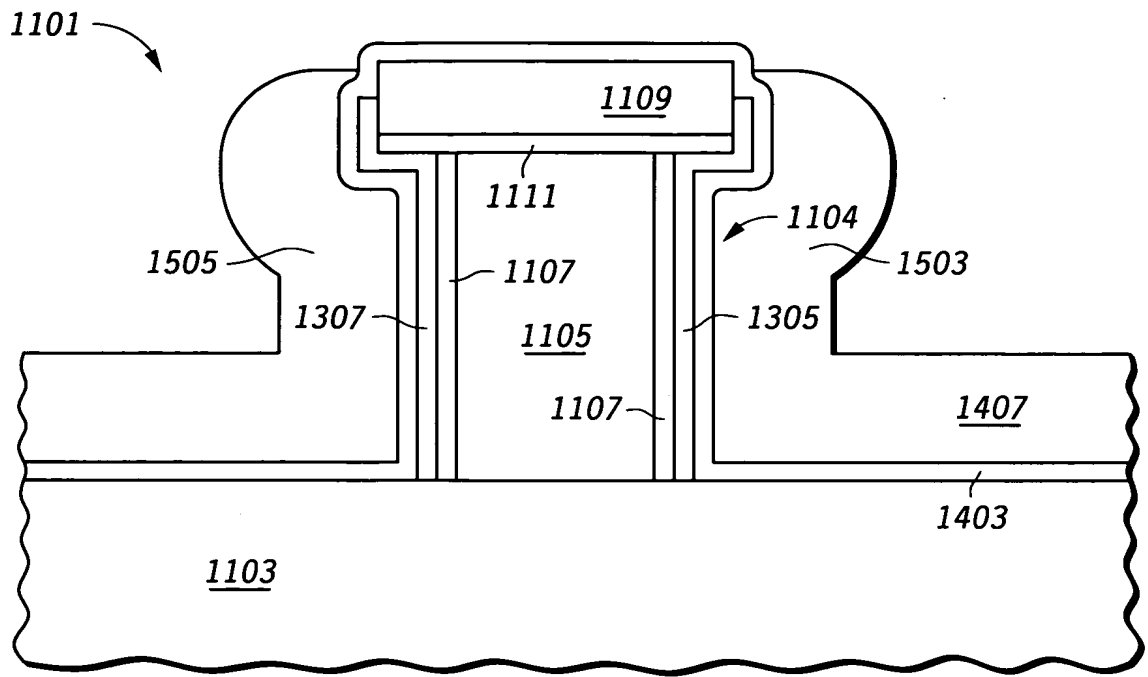


FIG. 15

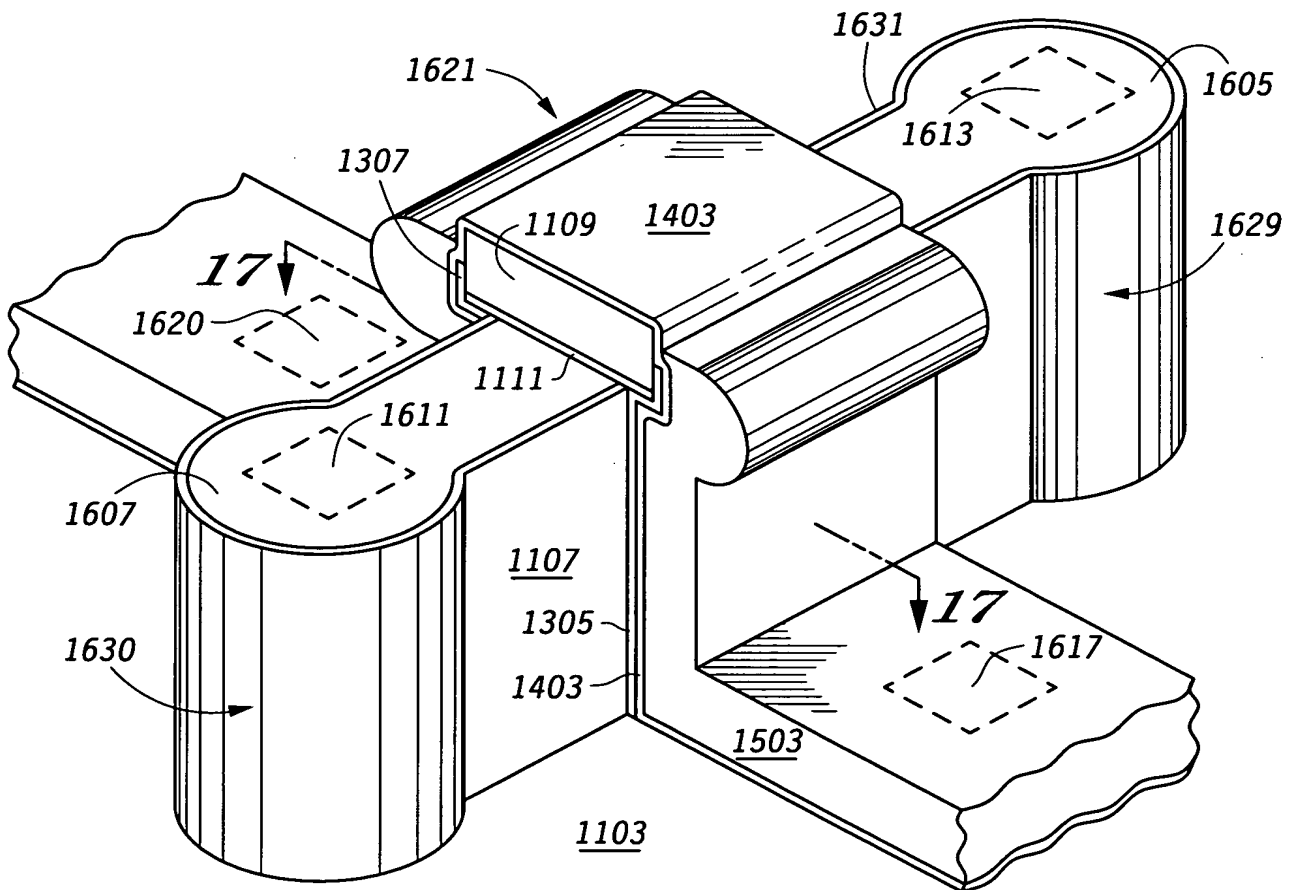


FIG. 16

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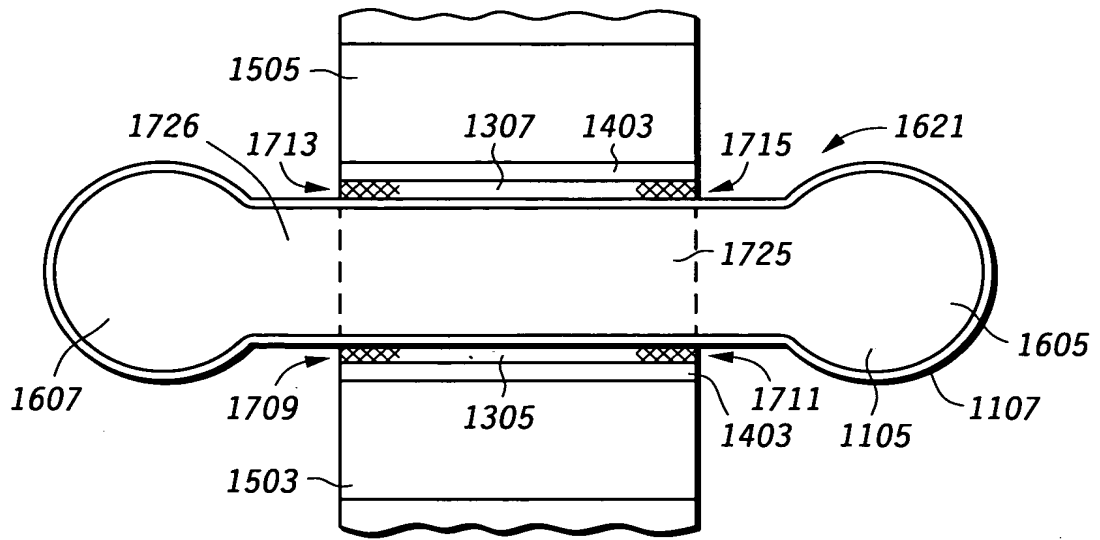


FIG. 17

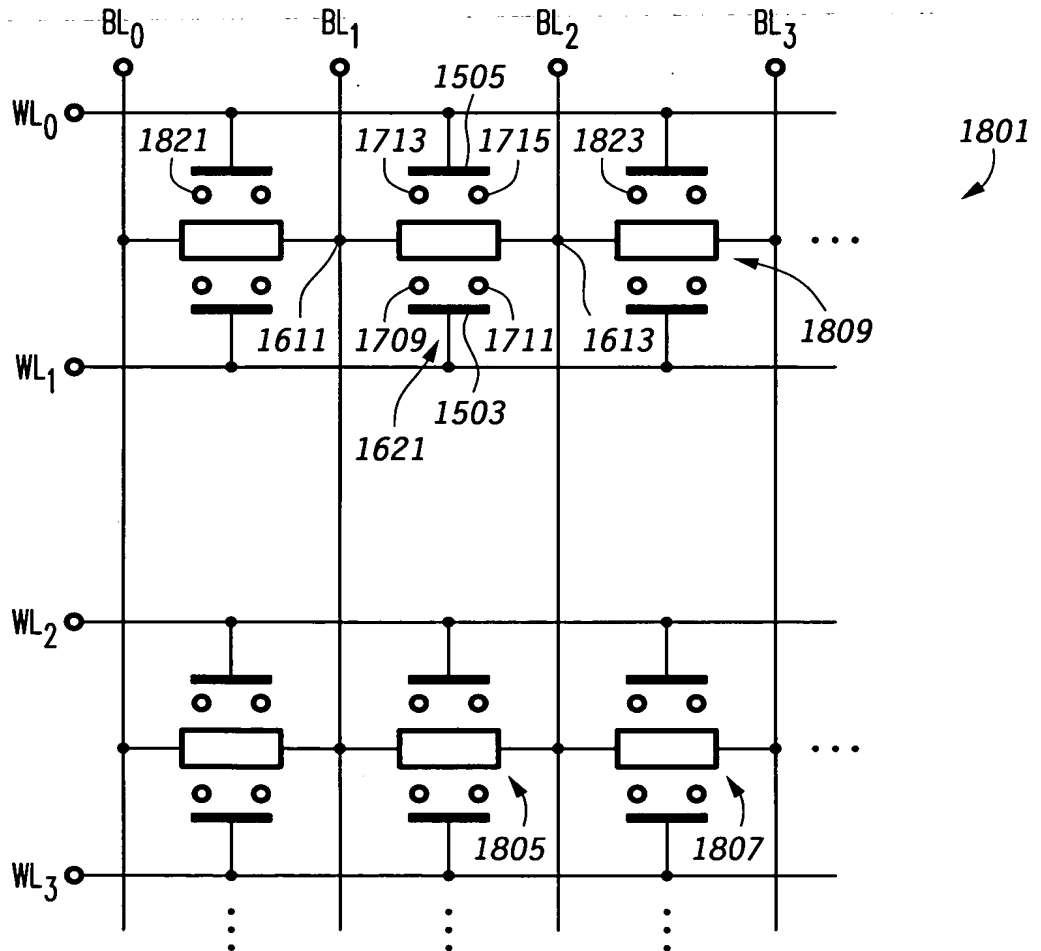


FIG. 18

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CONDITIONS FOR BIT 1713

	WL ₀	WL ₁	WL ₂	WL ₃	BL ₀	BL ₁	BL ₂	BL ₃
PROGRAM	V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{PP/2}	V _{PP/2}	V _{SS}	V _{SS}
ERASE	-V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{PP}	V _{SS}	V _{SS}
READ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	S _A	V _{DD}	V _{DD}

FIG. 19

CONDITIONS FOR BIT 1711

	WL ₀	WL ₁	WL ₂	WL ₃	BL ₀	BL ₁	BL ₂	BL ₃
PROGRAM	V _{SS}	V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{PP/2}	V _{PP/2}
ERASE	V _{SS}	-V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{PP}	V _{SS}
READ	V _{SS}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	S _A	V _{SS}

FIG. 20

	WL ₀	WL ₁	WL ₂	WL ₃	BL ₀	BL ₁	BL ₂	BL ₃
PROGRAM	V _{PP}	-V _{PP}	-V _{PP}	-V _{PP}	-V _{PP/2}	-V _{PP/2}	-V _{PP}	-V _{PP}
ERASE	-V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{PP}	V _{SS}	V _{SS}
READ	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	S _A	V _{DD}	V _{DD}

FIG. 21

	WL ₀	WL ₁	WL ₂	WL ₃	BL ₀	BL ₁	BL ₂	BL ₃
PROGRAM	-V _{PP}	V _{PP}	V _{PP}	V _{PP}	-V _{PP}	-V _{PP}	-V _{PP/2}	-V _{PP/2}
ERASE	V _{SS}	-V _{PP}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{PP}	V _{SS}
READ	V _{SS}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	S _A	V _{SS}

FIG. 22

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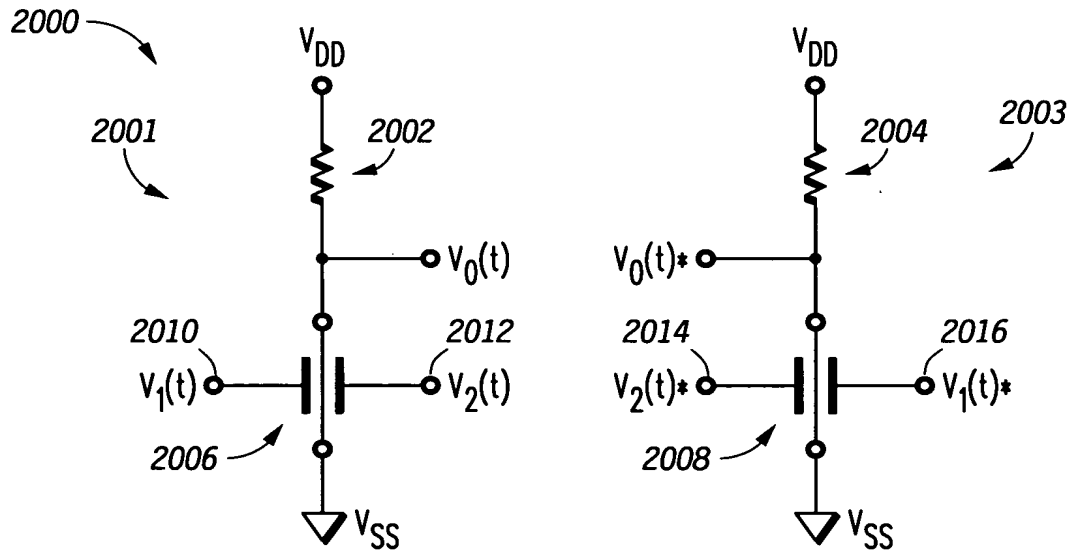


FIG. 23

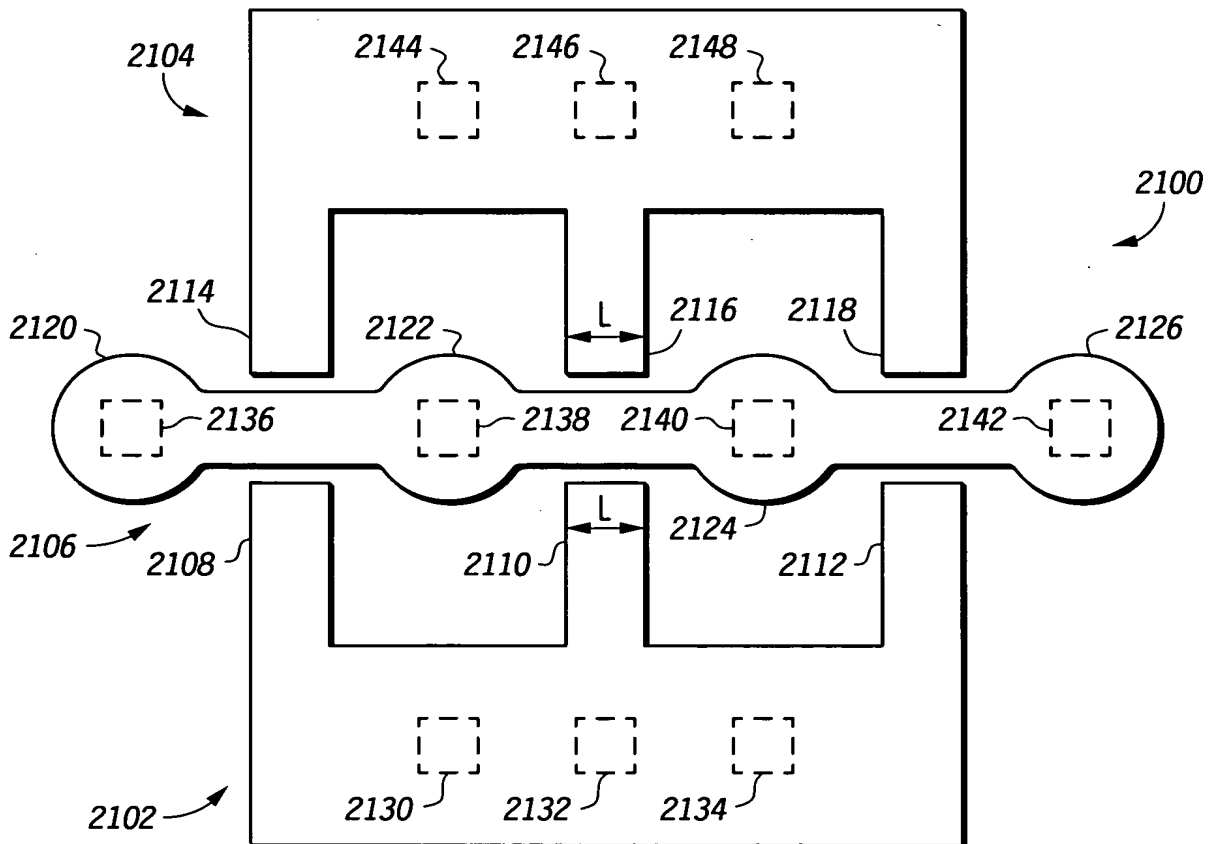


FIG. 24